PAPER-I
COMPUTER ORGANIZATION AND ARCHITECTURE
SUBJECT CODE: BCS-302

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief. **2 x 10 = 20**

Q. No.	Question	Marks	CO
a	List and define the main structural components of a computer.	2	1
b	What do you mean by bus arbitration? List different types of bus arbitration.	2	1
c	Explain the biasing with reference to floating point representation.	2	2
d	What is restoring division algorithm?	2	2
e	Write a short note on RISC.	2	3
f	Explain one, two and three address instruction.	2	3
g	What is hit ratio?	2	4
h	Why the auxiliary storage is organized in records or blocks?	2	4
i	What is the function of I/O interface?	2	5
j	What is an interrupt?	2	5

SECTION B

2. Attempt any three of the following: **10 x 3 = 30**

Q. No.	Question	Marks	CO
a.	Explain the diagram of bus system using multiplexer which has four registers of size 4-bits each.	10	1
b.	Explain in detail the principle of carry look ahead adder.	10	2
c.	What is micro program sequencer? Explain the working of micro program sequencer with block diagram.	10	3
d.	Explain the concept of memory. Describe the memory hierarchy in computer system.	10	4
e.	Explain the various modes of data transfer.	10	5

SECTION C

3. Attempt any one part of the following: **10 x 1 = 10**

Q. No.	Question	Marks	CO
a.	What is processor organization? Explain the various types of processor organization?	10	1
b.	Explain the advantages and disadvantages of polling and daisy chaining bus arbitration schemes.	10	1

4. Attempt any one part of the following: **10 x 1 = 10**

Q. No.	Question	Marks	CO
a.	Explain IEEE standard for floating point representation. Represent the number $(1460.125)_{10}$ in single precision and double precision format.	10	2
b.	Explain the Booth algorithm in detail with the help of flow chart. Give an example of multiplication using Booth`s algorithm.	10	2

5. Attempt any one part of the following: **10 x 1 = 10**

Q. No.	Question	Marks	CO
a.	Evaluate the arithmetic statement X=(A+B)*(C+D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression.	10	3
b.	Explain all the phases of instruction cycle	10	3

6. Attempt any one part of the following: **10 x 1 = 10**

Q. No.	Question	Marks	CO
a.	Explain the concept of cache memory. Explain the design issues in cache design.	10	4
b.	A computer uses RAM chips of 1024*1 capacity. (i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024*8? (ii) How many chips are needed to provide a memory capacity of 16 KB?	10	4

7. Attempt any one part of the following: **10 x 1 = 10**

Q. No.	Question	Marks	CO
a.	Explain about the DMA controller and its mode of data transfer in detail.	10	5
b.	Explain the difference between vectored and non-vectored interrupt. Give the examples of each.	10	5